THAT WHICH IS CLAIMED IS:

1. A decoding circuit (200) to decode a biphase signal (DALIIN0), said circuit comprising:

a precharging register (210) to precharge a pair of states of the biphase signal, a state of the pair of states being precharged at each pulse of a periodic precharging signal (PREC), and

a verification circuit (220) to compare the two states of the pair of states and give an active error signal (ER) if the two states are equal.

2. A circuit according to claim 1, wherein the verification circuit (200) also gives a decoded signal (OUT) representing the pair of states stored in the precharging register (210).

3. A circuit according to claim 2, also comprising a storage circuit (230), to store the decoded signal (OUT) at each pulse of a periodic validation signal (VAL), with a period equal to twice the period of the precharging signal (PREC).

4. A circuit according to one of the claims 1 to 3, also comprising a delay circuit (240), this delay circuit producing an end signal (FIN) after a predefined time to indicate the end of the biphase signal (DALIIN0), the delay circuit (240) being initialized at the beginning of the biphase signal (DALIIN0).

5. A circuit according to one of the above claims, also comprising a filter (250) to filter the biphase signal (DALIIN0), the filter (250) comprising an input to which the biphase signal (DALIIN0) is applied and an output connected to the serial input of the precharging register (210).

6. A method for the decoding of a biphase signal (DALIIN0) comprising:

a step for the precharging of a pair of states of the biphase signal, one state of the pair of states being precharged at each pulse of a periodic precharging signal (PREC),

a step for the comparison of the two states of the precharged pair of states, and

a step for supplying an error signal (ER) that is active if the two states are equal or inactive if not.

7. A method according to claim 6, also comprising a step for supplying a decoded signal (OUT) representing the precharged pair of states.

8. A method according to claim 7, also comprising a step for the storage of the decoded signal (OUT) at each pulse of a periodic validation signal (VAL), with a period equal to twice the period of the precharging signal (PREC).

9. A method according to one of the claims 6 to 8, also comprising a time measurement step, initialized at the start of the biphase signal (DALIIN0), to produce an end signal (FIN) after a predefined time, indicating the end of the biphase signal (DALIIN0).

10. A method according to one of the claims 6 to 9, also comprising a step for the filtering of the biphase signal (DALIIN0) performed before the precharging step.

11. A circuit for the transmission and reception of biphase signals encoded according to a DALI communications protocol, wherein the circuit comprises a

decoding circuit according to one of the claims 1 to 5.

12. A circuit for the control of an electronic ballast receiving driving signals in the form of biphase signals encoded according to the DALI communications protocol, wherein the circuit comprises a decoding circuit (200) according to one of the claims 1 to 5.